IN THE CLAIMS:

1. (Currently Amended) A method of manufacturing a semiconductor component comprising:

providing a delta-doped heteroepitaxial semiconductor structure substrate with a surface;

providing a layer of undoped gallium arsenide on the surface of the delta-doped heteroepitaxial semiconductor structure substrate, the layer having ~~comprising~~ a thickness ~~of at least~~ on the order of six to ~~approximately~~ twelve nanometers ~~of undoped gallium arsenide over the surface of the substrate~~;

forming a gate contact ~~over~~ on a first portion of the undoped gallium arsenide layer; and

removing a second portion of the undoped gallium arsenide layer to expose a portion of the surface of the delta-doped heteroepitaxial semiconductor structure substrate, wherein the remaining first portion of ~~said~~ the undoped gallium arsenide layer does not substantially extend beyond the horizontal profile of ~~said~~ the gate contact.

2. (Currently Amended) The method of claim 1 wherein:

~~said~~ the undoped gallium arsenide layer further comprises a thickness on the order of ~~at least~~ six to ~~approximately~~ nine nanometers of undoped gallium arsenide.

3. (Canceled)

4. (Currently Amended) The method of claim 1 wherein:

forming the gate contact ~~further comprises~~ includes exposing the second portion of the undoped gallium arsenide layer.

5. (Canceled)

6. (Currently Amended) The method of claim 1 further comprising:

implanting source and drain regions into the delta-doped heteroepitaxial semiconductor structure substrate after removing the second portion of the undoped gallium arsenide layer, wherein the first portion of the undoped gallium arsenide layer remains undoped.

7. (Currently Amended) The method of claim 1 further comprising:
implanting source and drain regions into the delta-doped heteroepitaxial semiconductor structure substrate before removing the second portion of the undoped gallium arsenide layer, wherein the first portion of the undoped gallium arsenide layer remains undoped.

8. (Currently Amended) The method of claim 1 further comprising:
forming a spacer adjacent to the gate contact after removing the second portion of the undoped gallium arsenide layer.

9. (Currently Amended) The method of claim 1 further comprising:
forming a spacer adjacent to the gate contact before removing the second portion of the undoped gallium arsenide layer.

10. (Currently Amended) The method of claim 9 further comprising:
keeping a third portion of the undoped gallium arsenide layer underneath the spacer after removing the second portion of the layer.

11. (Canceled)

12. (Currently Amended) The method of claim 1, wherein ~~wherein:~~
~~providing~~ the delta-doped heteroepitaxial semiconductor structure substrate ~~further~~ ~~comprises~~ includes:
~~providing~~ a semi-insulating gallium arsenide support layer;
~~providing~~ a buffer layer overlying the support layer, the buffer layer having a thickness on the order of one hundred to three hundred nanometers;
~~providing~~ a doping layer overlying the buffer layer;
~~providing~~ a spacer layer overlying the doping layer, the spacer layer having a thickness on the order of two to four nanometers;
~~providing~~ a channel layer overlying the spacer layer, the channel layer having a thickness on the order of ten to twenty nanometers; and
~~providing~~ a barrier layer overlying the channel layer, the barrier layer having a thickness on the order of fifteen to thirty-five nanometers.

13. (Canceled)

14. (Currently Amended) The method of claim 1 further comprising:

forming a dielectric layer over the gate contact, the remaining first portion of the undoped gallium arsenide layer and the exposed portion of the surface of the delta-doped heteroepitaxial semiconductor structure substrate, the dielectric layer having a thickness on the order of twenty to sixty nanometers;

implanting source and drain regions through the dielectric layer and into the surface of the delta-doped heteroepitaxial semiconductor structure substrate, the implant regions extending from the surface of the delta-doped heteroepitaxial semiconductor structure substrate into a buffer layer of the substrate but not extending into a support layer of the substrate, wherein the first portion of the undoped gallium arsenide layer remains undoped;

annealing the source and drain regions ~~after removing the second portion of the layer,~~ wherein annealing activates dopants in the implanted source and drain regions and increases a density of the dielectric layer; and

forming source and drain contacts over the source and drain regions ~~after removing the second portion of the layer~~ in respective source and drain contact vias, the source and drain contact vias extending through the dielectric layer and extending from the surface of the delta-doped heteroepitaxial semiconductor structure substrate into the buffer layer of the substrate but not extending into the support layer of the substrate.

15. (Canceled)

16. (Currently Amended) A method of manufacturing a semiconductor component comprising:

providing a delta-doped, heteroepitaxial semiconductor substrate with a surface, the delta-doped, heteroepitaxial semiconductor substrate comprising:

a support layer comprised of semi-insulating gallium arsenide;

a buffer layer comprised of undoped gallium arsenide overlying the support layer, the buffer layer having a thickness on the order of 100 - 300 nanometers;

a doping layer delta-doped with silicon and overlying the buffer layer;

a spacer layer comprised of undoped gallium arsenide and overlying the doping layer, the spacer layer having a thickness on the order of 2-4 nanometers;

a channel layer comprised of indium gallium arsenide and overlying the spacer layer, the channel layer having a thickness on the order of 10-20 nanometers; and

a barrier layer comprised of aluminum gallium arsenide and overlying the channel layer, the barrier layer having a thickness on the order of 15-35 nanometers and forming the surface for the delta-doped, heteroepitaxial semiconductor substrate;

providing an undoped gallium arsenide capping layer ~~having a thickness of at least six to approximately twelve nanometers and overlying~~ on the surface of the delta-doped, heteroepitaxial semiconductor substrate, the capping layer having a thickness on the order of 6-12 nanometers;

forming a gate contact ~~over~~ on the undoped gallium arsenide capping layer, the gate contact covering a first portion of the undoped gallium arsenide capping layer and being absent over a second portion of the undoped gallium arsenide capping layer;

removing the second portion of the undoped gallium arsenide capping layer after forming the gate contact to expose a portion of the surface of the delta-doped, heteroepitaxial semiconductor substrate, wherein the remaining first portion of said undoped gallium arsenide capping layer does not substantially extend beyond the horizontal profile of said gate contact;

forming a spacer adjacent to the gate contact;

forming source and drain regions in the delta-doped, heteroepitaxial semiconductor substrate; and

forming source and drain contacts over the source and drain regions ~~after removing the second portion of the undoped gallium arsenide capping layer~~ in respective source and drain contact vias, the source and drain contact vias extending through the dielectric layer and extending from the surface of the delta-doped heteroepitaxial semiconductor substrate into the buffer layer of the substrate but not extending into the support layer of the substrate.

17. (Currently Amended) The method of claim 16 wherein:

forming the source and drain regions further comprises implanting the source and drain regions through the dielectric layer and into the surface of the delta-doped, heteroepitaxial semiconductor substrate after removing the second portion of the undoped gallium arsenide capping layer, the implant regions extending from the surface of the delta-doped heteroepitaxial semiconductor substrate into a buffer layer of the substrate but not extending into a support layer of the substrate, wherein the first portion of the undoped gallium arsenide layer remains undoped; and

forming the spacer further comprises forming a multi-layered spacer adjacent to the gate contact after removing the second portion of the undoped gallium arsenide capping layer.

18. (Currently Amended) The method of claim 16 further comprising:

forming the source and drain regions further comprises implanting source and drain regions through the dielectric layer and into the surface of the delta-doped, heteroepitaxial semiconductor substrate before removing the second portion of the undoped gallium arsenide capping layer, the implant regions extending from the surface of the delta-doped heteroepitaxial semiconductor structure substrate into a buffer layer of the substrate but not extending into a support layer of the substrate, wherein the first portion of the undoped gallium arsenide layer remains undoped;

forming the spacer further comprises forming a multi-layered spacer adjacent to the gate contact before removing the second portion of the undoped gallium arsenide capping layer; and

keeping a third portion of the undoped gallium arsenide capping layer underneath the multi-layered spacer after removing the second portion of the undoped gallium arsenide capping layer.

19. (Currently Amended) The method of claim 16 wherein:

providing the undoped gallium arsenide capping layer further comprises providing the undoped gallium arsenide capping layer with a thickness on the order of ~~at least~~ six to ~~approximately~~ nine nanometers.

20. (Original) The method of claim 16 wherein:

providing the delta-doped, heteroepitaxial semiconductor substrate further comprises:

providing the buffer layer on the support layer and consisting essentially of gallium arsenide;

providing the doping layer on the buffer layer and consisting essentially of silicon and gallium arsenide;

providing the spacer layer on the doping layer and consisting essentially of gallium arsenide;

providing the channel layer on the spacer layer and consisting essentially of indium gallium arsenide; and

providing the barrier layer on the channel layer and consisting essentially of aluminum gallium arsenide;

providing the undoped gallium arsenide capping layer further comprises:

providing the undoped gallium arsenide capping layer on the barrier layer;

forming the gate contact further comprises:

forming the gate contact on the first portion of the undoped gallium arsenide capping layer; and

removing the second portion of the undoped gallium arsenide capping layer further comprises:

removing the second portion of the undoped gallium arsenide capping layer to expose a portion of the barrier layer.

21. (Original) The method of claim 20 further comprising:

annealing the source and drain regions after removing the second portion of the undoped gallium arsenide capping layer,

wherein:

providing the undoped gallium arsenide capping layer further comprises

providing the undoped gallium arsenide capping layer with a thickness of approximately six to nine nanometers.

22. (Previously Withdrawn) A semiconductor component comprising:
a substrate with a surface;
a layer comprised of undoped gallium arsenide over a first portion of the surface of the substrate; and
a gate contact over the layer,
wherein:
the layer is absent over a second portion of the substrate.

23. (Previously Withdrawn) The semiconductor component of claim 22 wherein:
the layer has a thickness of approximately six to nine nanometers.

24. (Previously Withdrawn) The semiconductor component of claim 22 wherein:
the layer has a thickness of approximately three to twelve nanometers; and
the substrate is a delta-doped, heteroepitaxial semiconductor substrate comprising:
a support layer comprised of semi-insulating gallium arsenide;
a buffer layer comprised of gallium arsenide overlying the support layer;
a doping layer delta-doped with silicon and overlying the buffer layer;
a spacer layer comprised of gallium arsenide and overlying the doping layer;
an channel layer comprised of indium gallium arsenide and overlying the spacer layer; and
a barrier layer comprised of aluminum gallium arsenide and overlying the channel layer, the barrier layer forming the surface for the delta-doped, heteroepitaxial semiconductor substrate.

25. (Previously Withdrawn) The semiconductor component of claim 24 further comprising:
source and drain regions in the substrate;
a multi-layered spacer adjacent to the gate contact; and
source and drain contacts overlying the source and drain regions.